GP 2814

PATENT
ATTY. DKT. NO. AMAT-1931/MD/PVD/DV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fusen Chen et al. §

Serial No. 08/856,116 § Group Art Unit: 2814

Filed: May 14, 1997 § Examiner: Bernard Souw

For: Reliability Barrier Integration for CU Application §

CERTIFICATE OF MAILING
37 C.F.R. 1.8
I hereby certify that this correspondence is being deposited on March 2, 1999, with the U. S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231.
3/2/99 Keith M. Tackett
Date

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Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

RESPONSE TO RESTRICTION REQUIREMENT

In response to the Examiner's Action mailed February 4, 1999, having a one-month response period set to expire on March 4, 1999, Applicants provisionally elect claims 1-18 and 20, and request reconsideration of the restriction requirement for reasons discussed below.

THE CLAIMS

Sub B1

1. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:

a) depositing a generally conformal first barrier layer in the hole;

b) removing the first barrier layer formed on the bottom of the hole;

c) sputter depositing a second barrier layer under conditions of a high density plasma; and

d) depositing a metal layer in the hole.

2. The method of claim 1 wherein the first barrier layer is deposited using chemical vapor deposition techniques.

3. The method of claim 2 wherein the barrier layer is comprised of Si_xN_y.